GWU Test Structures
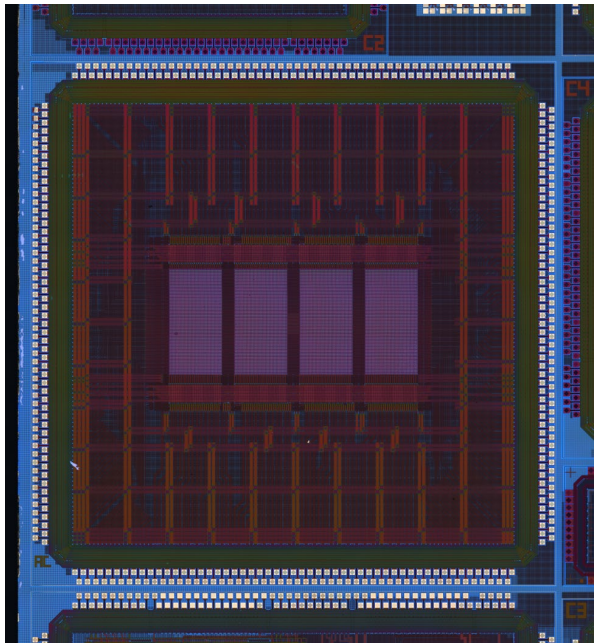## Nanotechnology Accelerator Platform

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PhD students involved: Lei Zhang, Imtiaz Hossen, Osama Yousuf, Joseph Riem

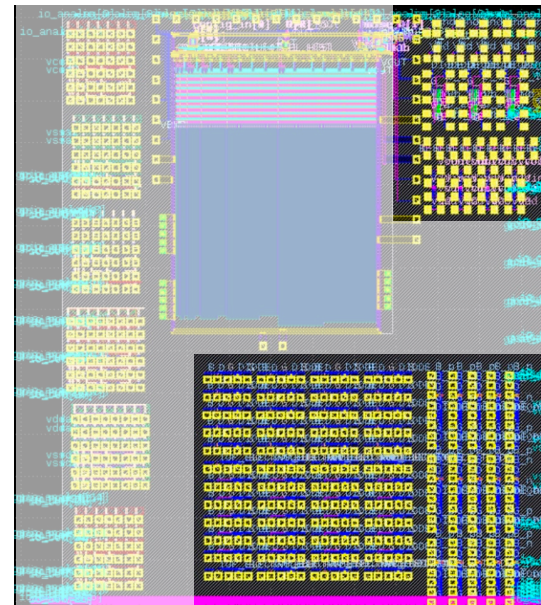# Summary of our contributions so far
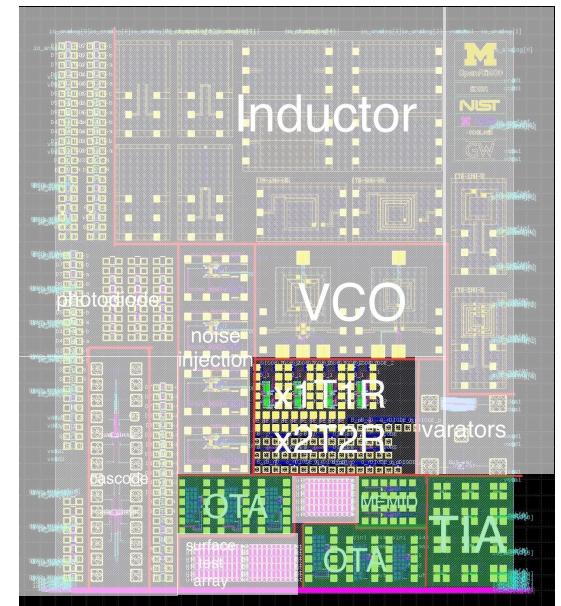
Device-level

• RRAM device integration

Circuit-level
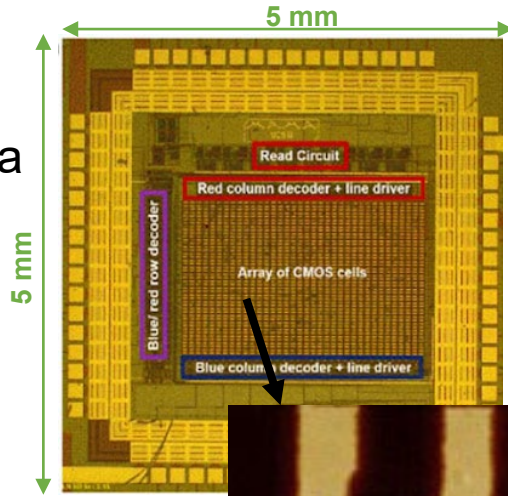
• Tape-outs in Sky130

MPW 6

MPW 7

+ System-level prototyping under way

Our experience with in-house RRAM/CMOS integration

Current approach
@ GWU and NIST
(~2021 – 2022)

**Prior approach**
@ UC Santa Barbara
(~2012 – 2016)

5 mm

5 mm

Read Circuit

Red column decoder + line driver

Blue red row decoder

Array of CMOS cells

Blue column decoder + line driver

Small chip
(difficult to handle in cleanroom)

10 mm

20 mm

Top   Bottom   3.2 µm 5 µm

Topography before
planarization
(unplanarized top metal as
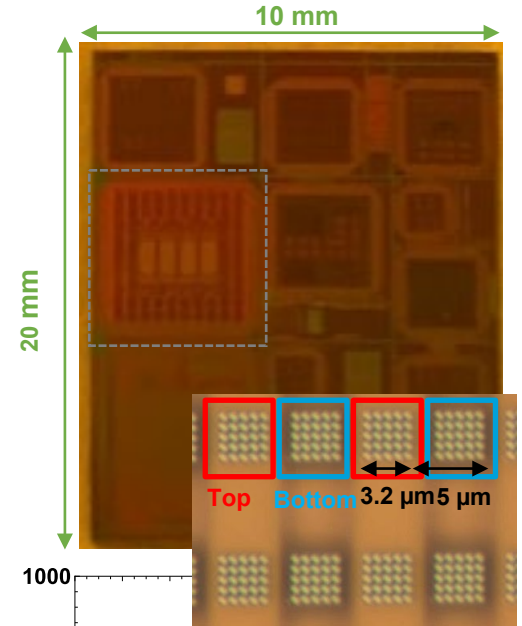received from foundry)

Topography after
planarization
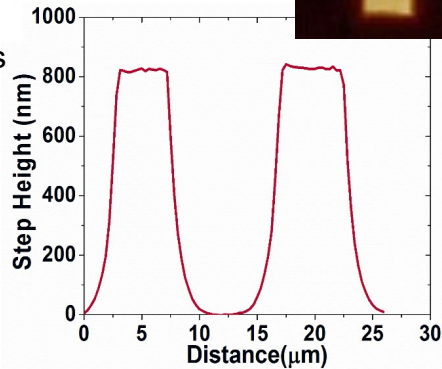
<10nm peak-to-valley

In-house
planarization
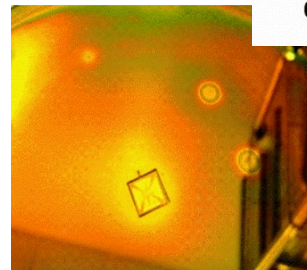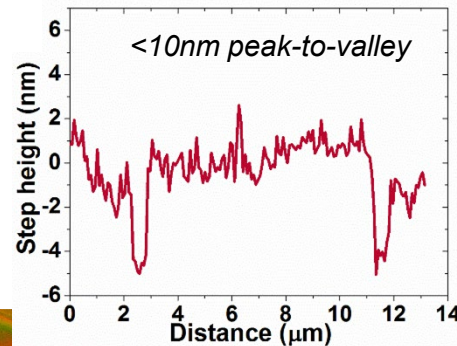
In-house fabricated RRAM connected to vias
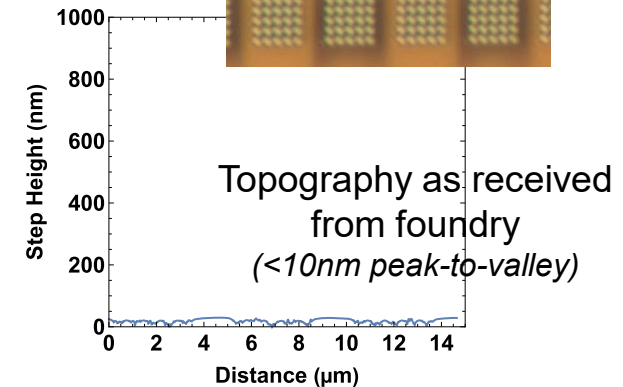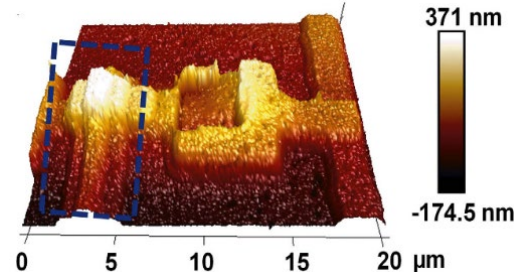
Topography as received
from foundry
(<10nm peak-to-valley)

371 nm

-174.5 nm

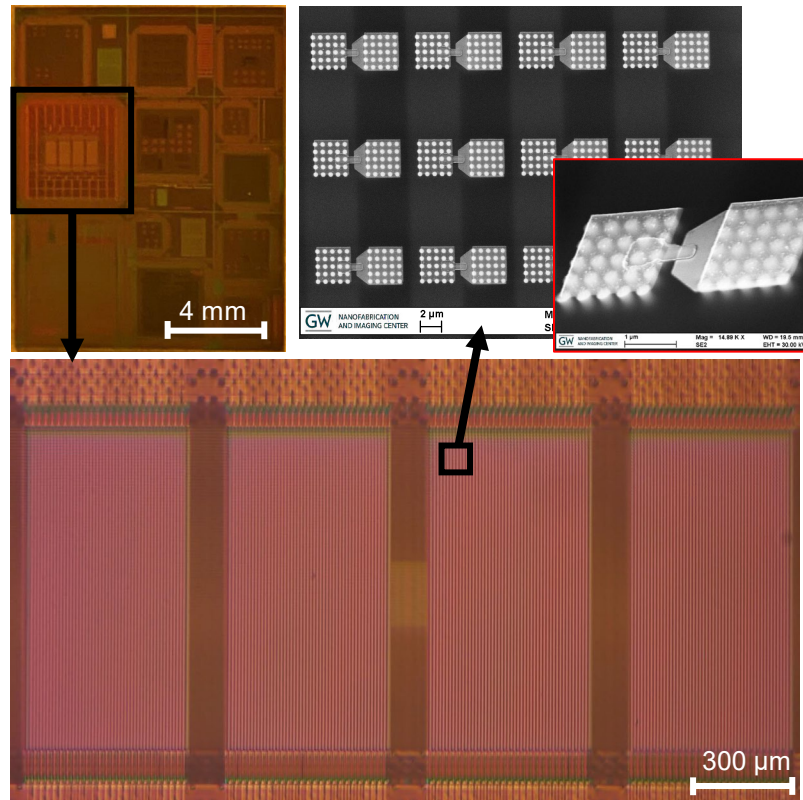*B. Chakrabarti et
al., Sci Rep **7**, 2017*

In-house fabricated
RRAM device
connected to vias
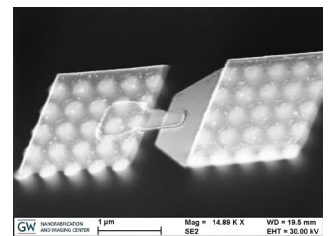
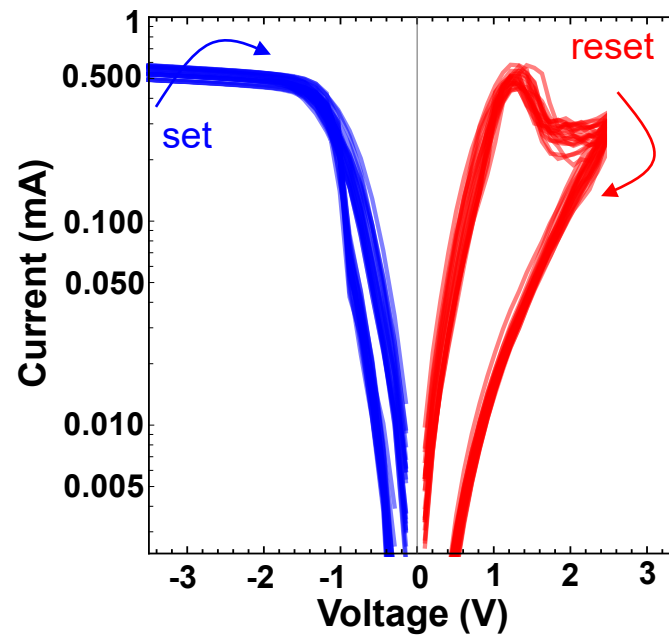# Current device-level integration

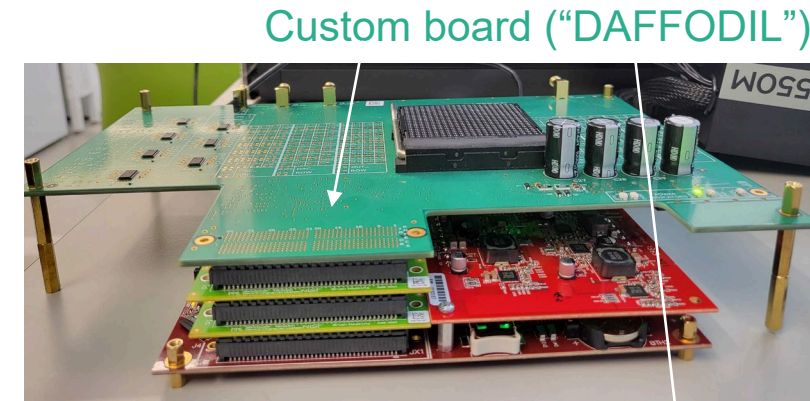- 20,000 RRAM devices integrated on CMOS in a 2T1R structure

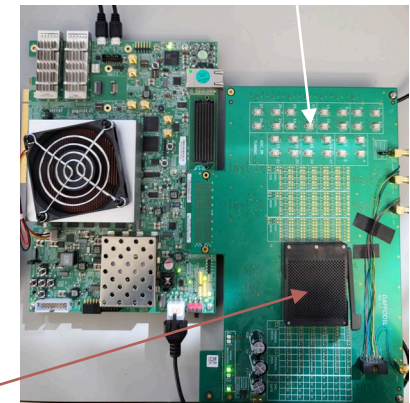**Fabrication**

accepted for invited talk at IEEE NMDC 2022

Testing

- current yield ~50%
- material stack engineering under way

System-level prototyping
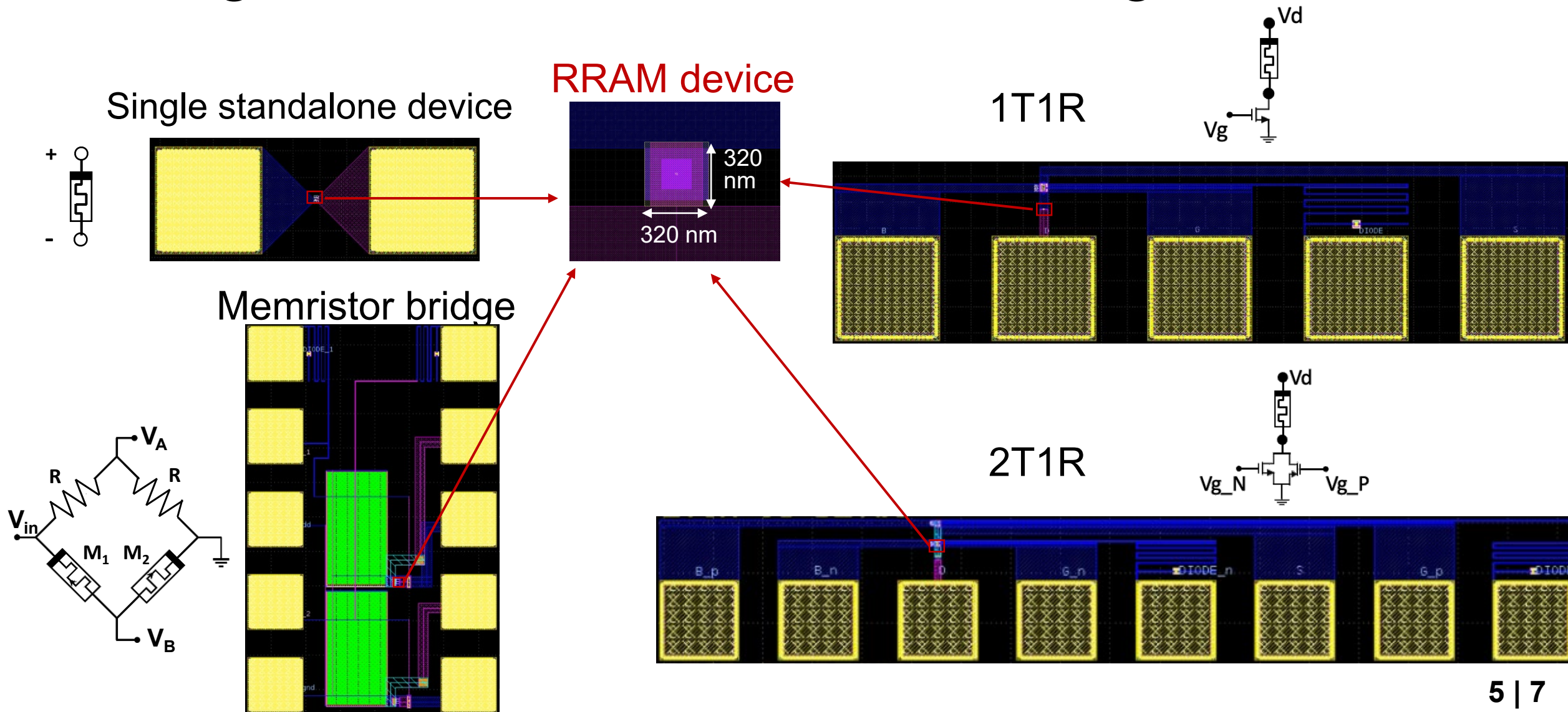
Custom board ("DAFFODIL")

support for different FPGA boards (that host a Linux OS)

slot for package with RRAM/CMOS chip

ICONS 2021, DARPA ERI 2020

Integrated circuits for RRAM testing

Single standalone device

RRAM device

1T1R

2T1R

Memristor bridge

320 nm

320 nm

Vd

Vg

Vd

Vg_N   Vg_P

Circuit units for distributed computing

- Building blocks
  - Pseudo-resistors
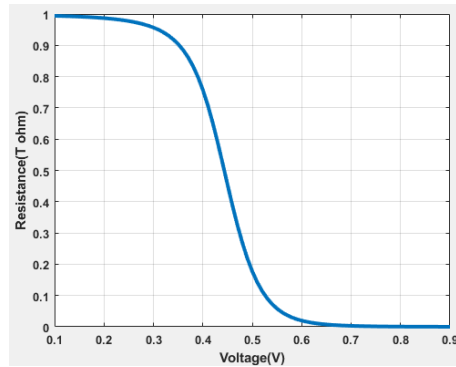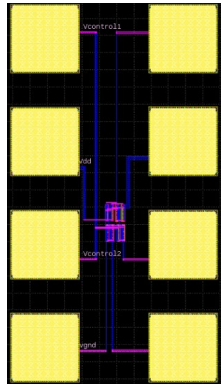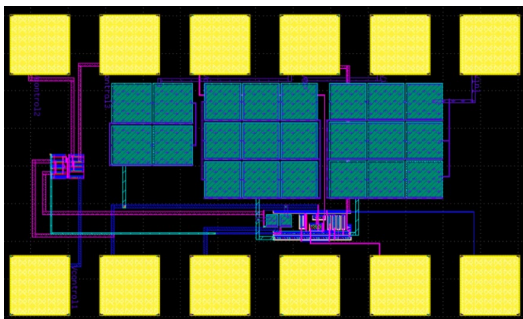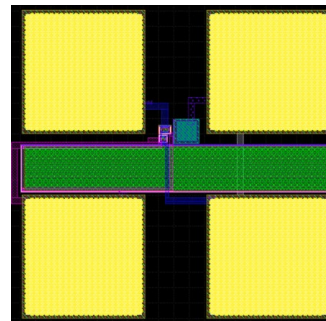

Resistance range: 130 MΩ to 1 TΩ

  - Low-frequency amplifiers
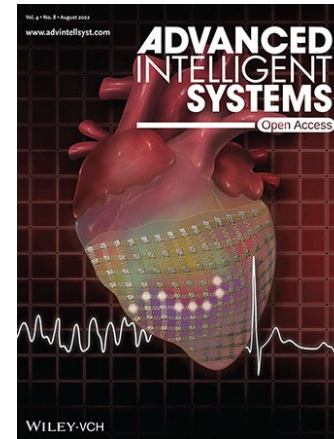
OTA

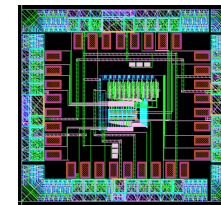Passband: 1.3Hz to 274.8Hz

TIA

Passband: 100mHz to 1GHz

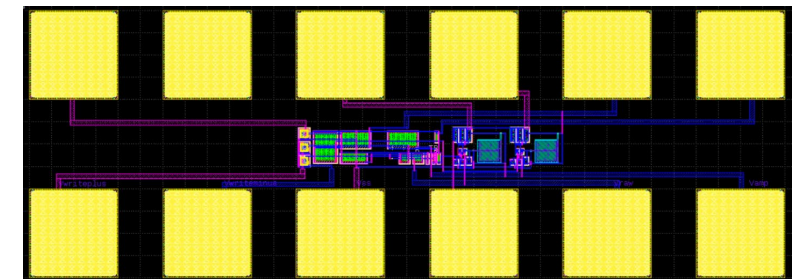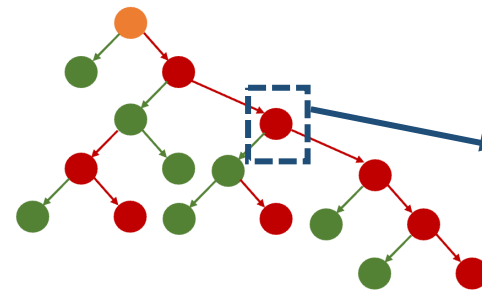- Circuit tiles for distributed computing
  - Cellular neural networks

Programmable chiplets for cardiac wavefront detection

  - Decision trees

CMOS/RRAM circuit for programmable decision tree leaf

decision tree structure for network intrusion detection

Thanks to collaborators:

Thanks to funding agencies: